Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A non-volatile memory comprising:

a plurality of memory blocks, each of the memory blocks comprising a plurality of word lines, each of the word lines being electrically connected to a plurality of memory cells;

a first decoder for decoding a memory address to generate a plurality of first decoding signals;

a second decoder for decoding the memory address to generate a plurality of second decoding signals; and

a row driver for driving a predetermined word line to approach a predetermined voltage level, the row driver comprising:

a plurality of word line drivers electrically connected to the first decoder and the second decoder, each of the word line drivers comprising:

a plurality of driving units, each of the driving units being electrically connected to a word line; and

a memory block selector electrically connected to the driving units for turning on the driving units according to the first decoding signals; and

a driving voltage output circuit electrically connected to

the driving units for determining a plurality of driving voltages according to the second decoding signals without using the first decoding signals, and outputting a predetermined driving voltage to drive the predetermined word line to approach the predetermined voltage level when a driving unit connected to the predetermined word line is turned on to electrically connect the predetermined word line and the driving voltage output circuit.

[c2] 2. The non-volatile memory of claim 1 being a flash memory.

[c3] 3. The non-volatile memory of claim 1 being fabricated through a complementary metal oxide semiconductor (CMOS) process.

[c4] 4. The non-volatile memory of claim 3 wherein each of the driving units comprises:
a PMOS transistor comprising:
a drain electrically connected to a driving voltage;
a source electrically connected to a word line; and
a gate electrically connected to a first output port of the memory block selector; and
a first NMOS transistor comprising:
a drain electrically connected to the source of the PMOS transistor;
a source electrically connected to a specific voltage; and

a gate electrically connected to a second output port of the memory block selector.

[c5] 5. The non-volatile memory of claim 4 wherein the PMOS transistor is formed on an n-type substrate, and the first NMOS transistor is formed on a p-type substrate.

[c6] 6. The non-volatile memory of claim 5 wherein the p-type substrate is electrically connected to the source of the first NMOS transistor, and the row driver further comprises a substrate voltage controller electrically connected to the n-type substrate for outputting a control voltage to the n-type substrate.

[c7] 7. The non-volatile memory of claim 6 wherein if the non-volatile memory runs a reading operation or a programming operation, the control voltage corresponds to a first voltage level, and if the non-volatile memory runs an erasing operation, the control voltage corresponds to a second voltage level.

[c8] 8. The non-volatile memory of claim 7 wherein the first voltage level is higher than the second voltage level.

[c9] 9. The non-volatile memory of claim 4 wherein each of the driving units further comprises a second NMOS transistor, and the second NMOS transistor comprises a drain electrically connected to the source of the PMOS

transistor, a source electrically connected to the specific voltage, and a gate.

[c10] 10. The non-volatile memory of claim 9 further comprising a word line reset circuit electrically connected to the gate of the second NMOS transistor for outputting a control voltage to the gate of the second NMOS transistor.

[c11] 11. The non-volatile memory of claim 10 wherein if the non-volatile memory runs an erasing operation, the control voltage outputted from the word line reset circuit is unable to turn on the second NMOS transistor.

[c12] 12. The non-volatile memory of claim 11 wherein the non-volatile memory runs a reading operation or a programming operation, and a word line associated with the driving unit is selected, the control voltage outputted from the word line reset circuit is unable to turn on the second NMOS transistor.

[c13] 13. The non-volatile memory of claim 4 wherein if the memory block selector selects the driving units, the first output port of the memory block corresponds to a first voltage to turn on the PMOS transistor, and if the memory block selector does not select the driving units, the first output port of the memory block corresponds to a

second voltage to turn off the PMOS transistor.

[c14] 14. The non-volatile memory of claim 4 wherein if the memory block selector selects the driving units, the second output port of the memory block corresponds to a first voltage to turn off the NMOS transistor, and if the memory block selector does not select the driving units, the second output port of the memory block corresponds to a second voltage to turn on the PMOS transistor.